FIG. 1

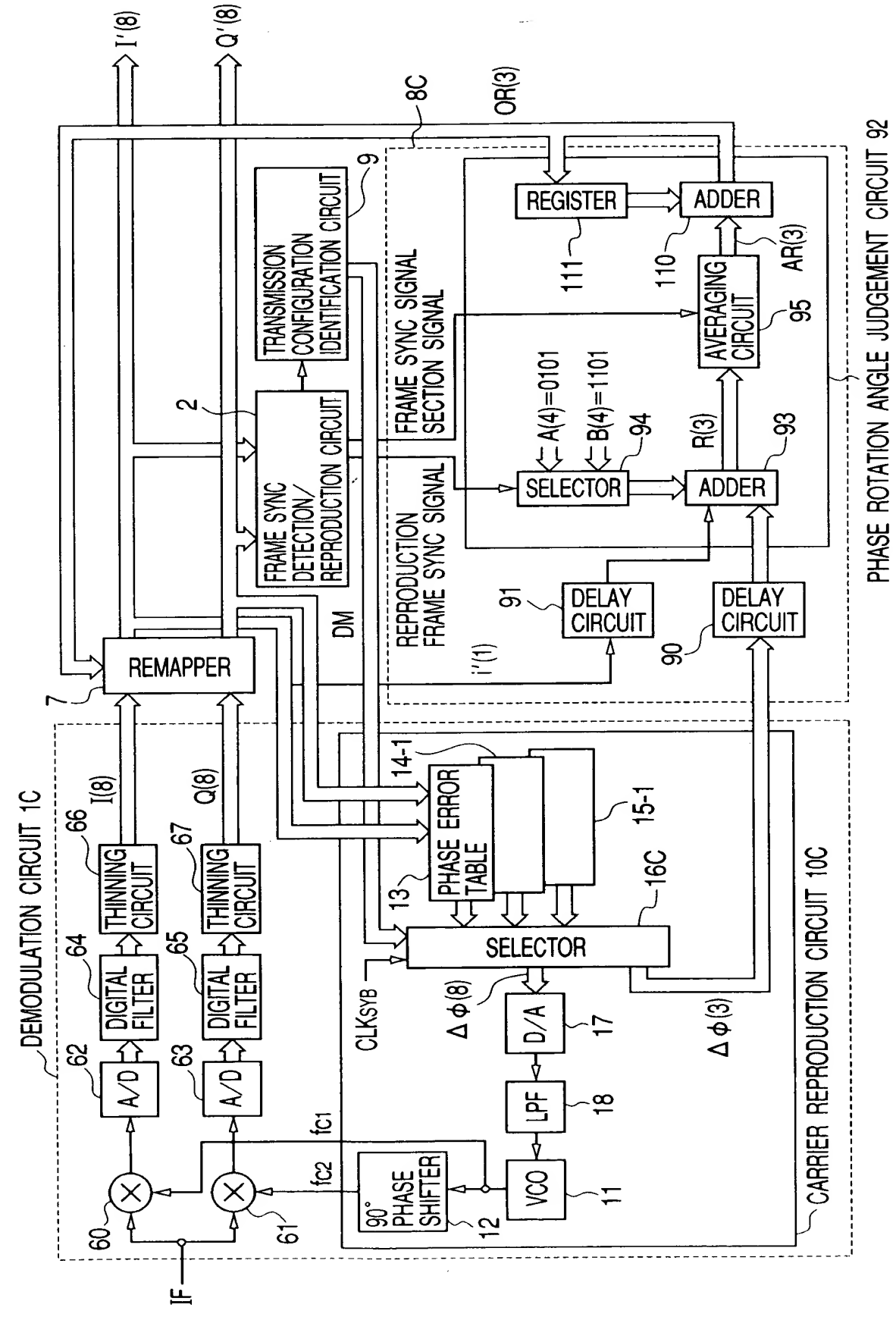

I'(8)
Q'(8)
8C
OR(3)
REGISTER
ADDER
111
110
AR(3)
AVERAGING CIRCUIT
95
TRANSMISSION CONFIGURATION IDENTIFICATION CIRCUIT
9
2
FRAME SYNC DETECTION/ REPRODUCTION CIRCUIT
FRAME SYNC SIGNAL SECTION SIGNAL
A(4)=0101
B(4)=1101
94
R(3)
93
SELECTOR
ADDER
REPRODUCTION FRAME SYNC SIGNAL
DM
91
DELAY CIRCUIT
90
DELAY CIRCUIT
i''(1)
PHASE ROTATION ANGLE JUDGEMENT CIRCUIT 92
REMAPPER
7
14-1
PHASE ERROR TABLE
15-1
13
16C
SELECTOR
I(8)
Q(8)
66
67
THINNING CIRCUIT
THINNING CIRCUIT
64
65
DIGITAL FILTER
DIGITAL FILTER
62
63
A/D
A/D
DEMODULATION CIRCUIT 1C
CLKSYB
Δφ(8)
D/A
17
Δφ(3)
LPF
18
fc1
fc2
90° PHASE SHIFTER
VCO
11
12
60
61
IF
CARRIER REPRODUCTION CIRCUIT 10C

FIG. 2A

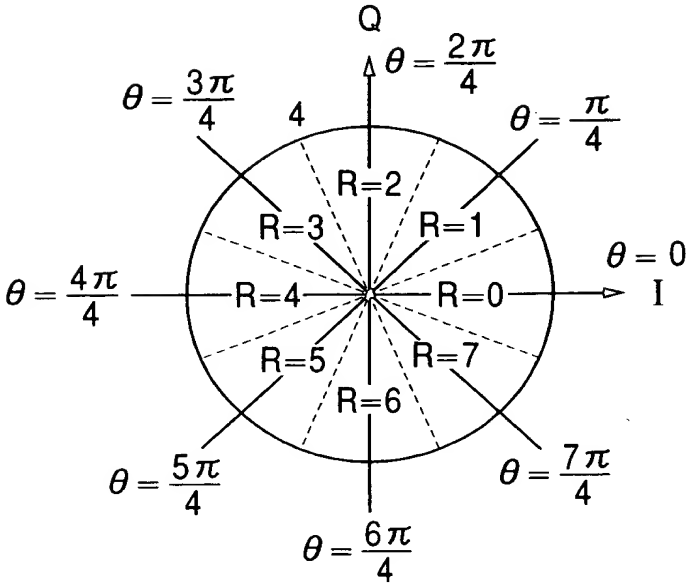


FIG. 2B

θ	R	R (3)
0	0	0 0 0
π/4	1	0 0 1
2π/4	2	0 1 0
3π/4	3	0 1 1
4π/4	4	1 0 0
5π/4	5	1 0 1
6π/4	6	1 1 0
7π/4	7	1 1 1

FIG. 3

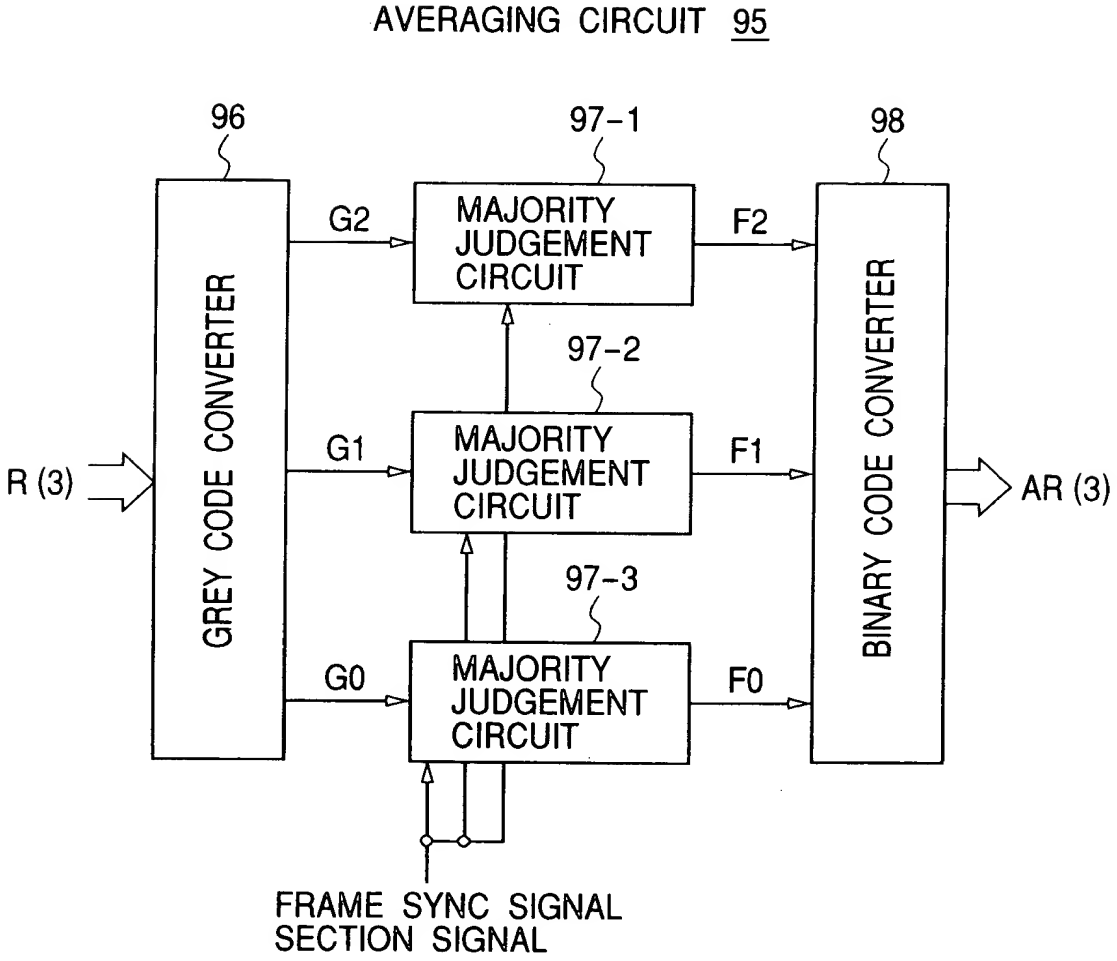

AVERAGING CIRCUIT 95
96
97-1
98
G2
MAJORITY JUDGEMENT CIRCUIT
F2
GREY CODE CONVERTER
BINARY CODE CONVERTER
97-2
R (3)
G1
MAJORITY JUDGEMENT CIRCUIT
F1
AR (3)
97-3
G0
MAJORITY JUDGEMENT CIRCUIT
F0
FRAME SYNC SIGNAL
SECTION SIGNAL

FIG. 4A

INPUT	OUTPUT
000	000
001	001
010	011
011	010
100	110
101	111
110	101
111	100

FIG. 4B

INPUT	OUTPUT
000	000
001	001
011	010
010	011
110	100
111	101
101	110
100	111

FIG. 5

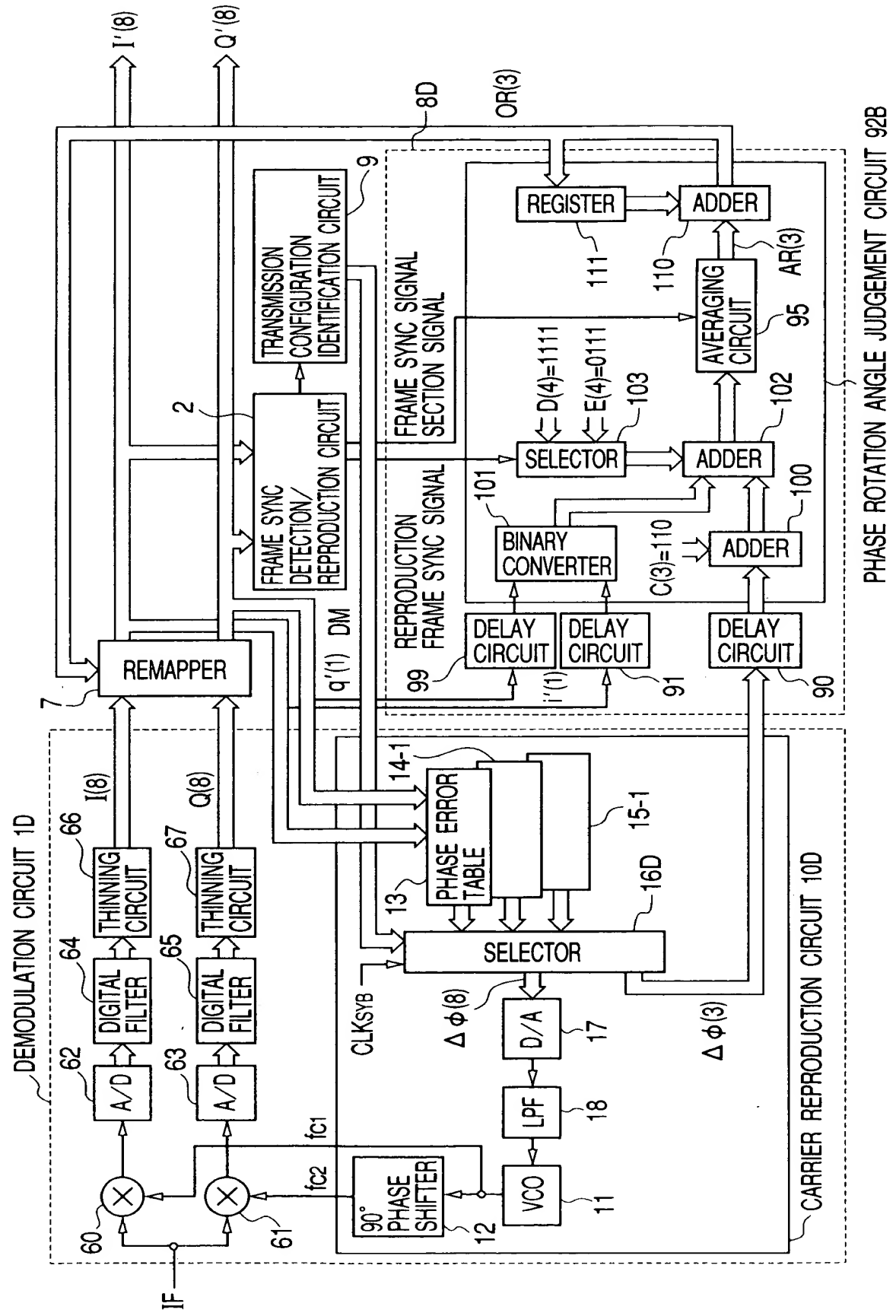

I'(8)
Q'(8)
8D
OR(3)
TRANSMISSION CONFIGURATION IDENTIFICATION CIRCUIT
9
FRAME SYNC DETECTION/ REPRODUCTION CIRCUIT
2
FRAME SYNC SIGNAL SECTION SIGNAL
REPRODUCTION FRAME SYNC SIGNAL
REGISTER
ADDER
111
110
AR(3)
AVERAGING CIRCUIT
95
D(4)=1111
E(4)=0111
103
SELECTOR
ADDER
102
101
BINARY CONVERTER
C(3)=110
ADDER
100
DELAY CIRCUIT
DELAY CIRCUIT
DELAY CIRCUIT
99
91
90
PHASE ROTATION ANGLE JUDGEMENT CIRCUIT 92B
REMAPPER
7
q'(1) DM
i'(1)
DEMODULATION CIRCUIT 1D
I(8)
Q(8)
66
67
THINNING CIRCUIT
THINNING CIRCUIT
64
65
DIGITAL FILTER
DIGITAL FILTER
62
63
A/D
A/D
14-1
PHASE ERROR TABLE
15-1
13
16D
SELECTOR
CLKSYB
Δφ(8)
D/A
17
LPF
18
VCO
11
fc1
fc2
90° PHASE SHIFTER
12
60
61
IF
Δφ(3)
CARRIER REPRODUCTION CIRCUIT 10D

FIG. 6

INPUT (q (1) i (1))	OUTPUT
0 0	0 0
0 1	0 1
1 1	1 0
1 0	1 1

FIG. 7

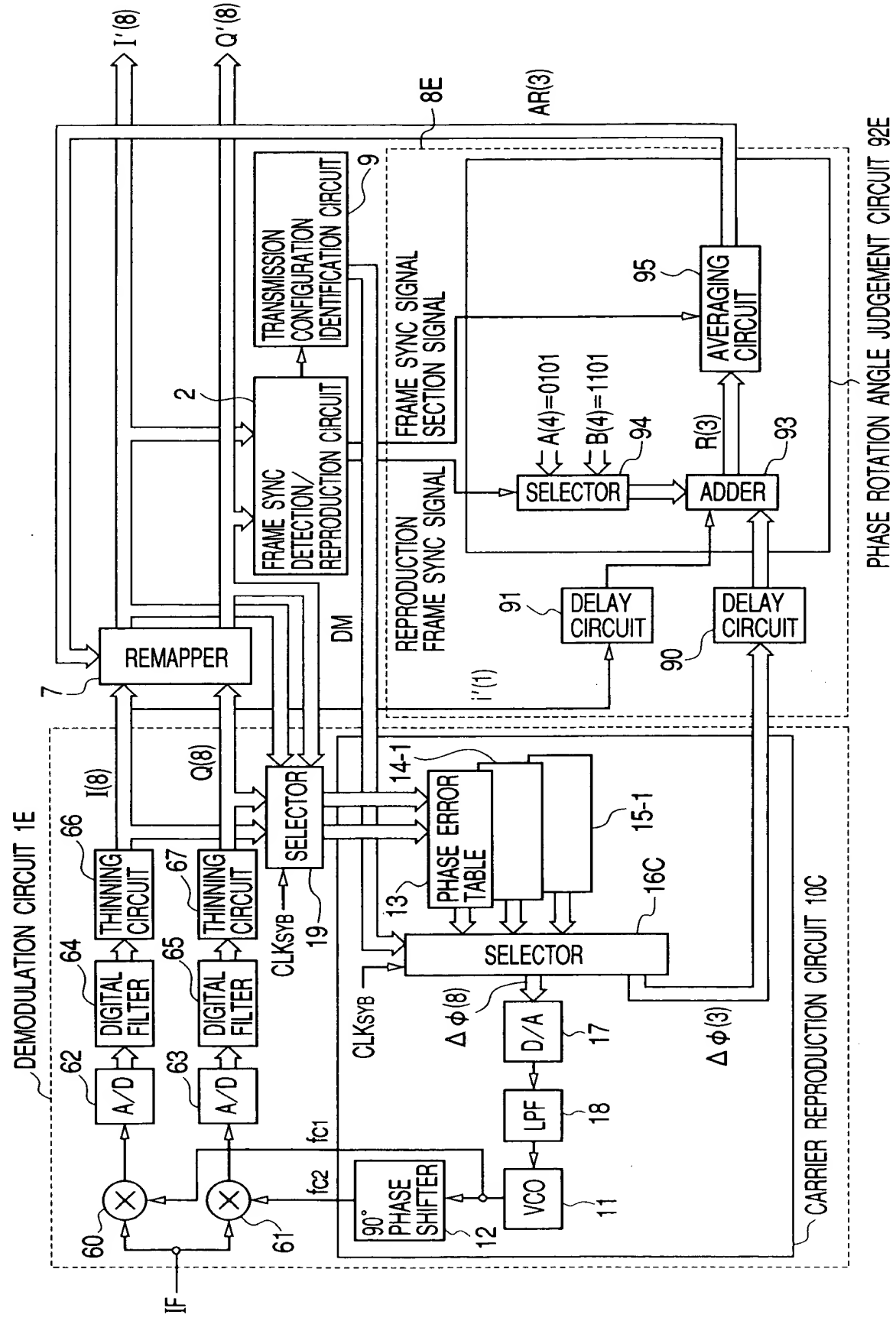

I'(8)
Q'(8)
8E
AR(3)
TRANSMISSION CONFIGURATION IDENTIFICATION CIRCUIT
9
FRAME SYNC DETECTION/ REPRODUCTION CIRCUIT
2
FRAME SYNC SIGNAL SECTION SIGNAL
REPRODUCTION FRAME SYNC SIGNAL
95
AVERAGING CIRCUIT
A(4)=0101
B(4)=1101
94
SELECTOR
R(3)
93
ADDER
PHASE ROTATION ANGLE JUDGEMENT CIRCUIT 92E
91
DELAY CIRCUIT
90
DELAY CIRCUIT
REMAPPER
7
DM
I'(1)
DEMODULATION CIRCUIT 1E
I(8)
Q(8)
SELECTOR
14-1
PHASE ERROR TABLE
15-1
13
16C
SELECTOR
CARRIER REPRODUCTION CIRCUIT 10C
66
THINNING CIRCUIT
67
THINNING CIRCUIT
64
DIGITAL FILTER
65
DIGITAL FILTER
CLKSYB
19
CLKSYB
Δφ(8)
D/A
17
Δφ(3)
62
A/D
63
A/D
LPF
18
fc1
fc2
90° PHASE SHIFTER
12
VCO
11
60
61
IF

FIG. 8

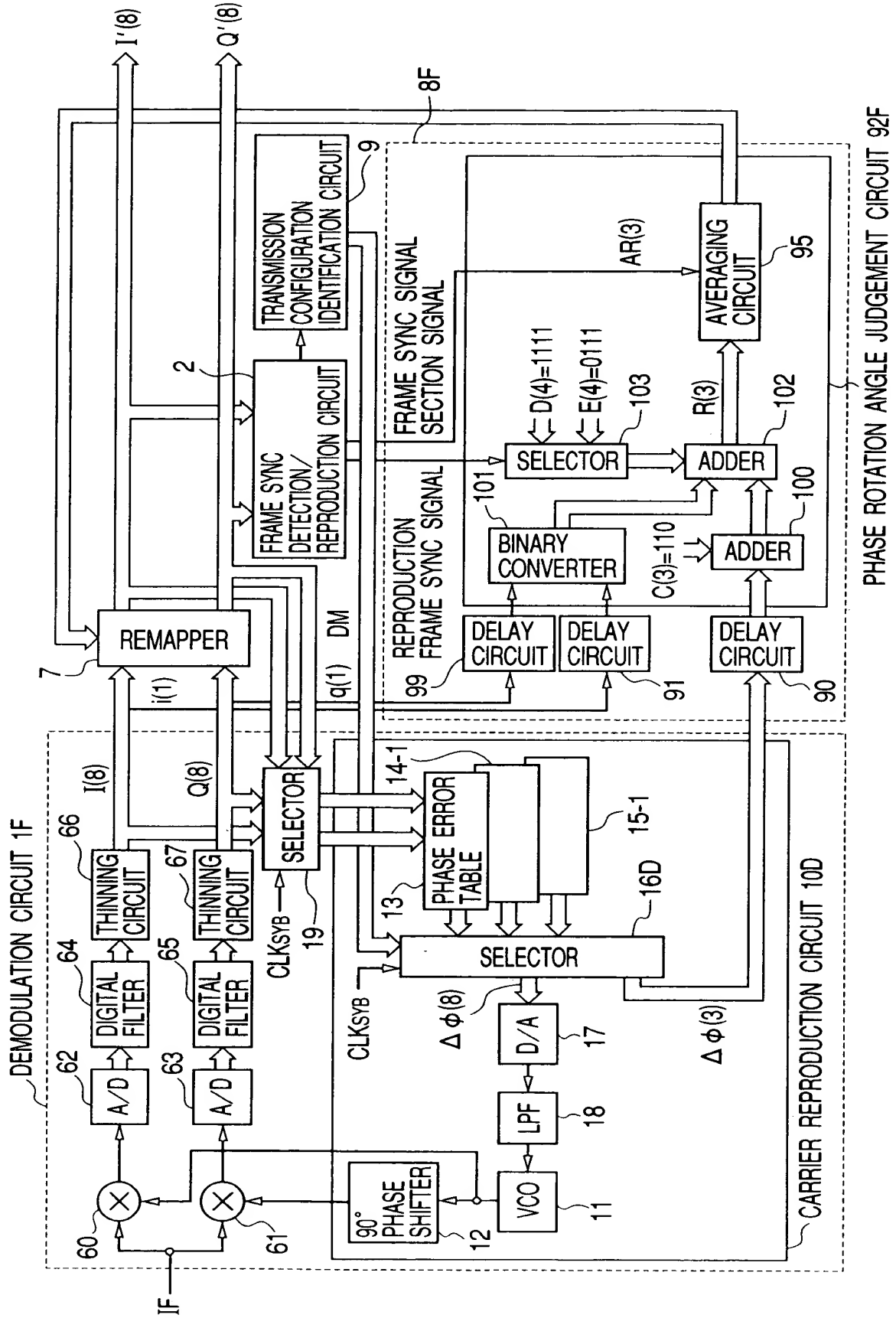

I'(8)
Q'(8)
8F
TRANSMISSION CONFIGURATION IDENTIFICATION CIRCUIT
9
2
FRAME SYNC DETECTION/ REPRODUCTION CIRCUIT
FRAME SYNC SIGNAL SECTION SIGNAL
REPRODUCTION FRAME SYNC SIGNAL
AR(3)
AVERAGING CIRCUIT
95
D(4)=1111
E(4)=0111
103
SELECTOR
R(3)
ADDER
102
101
BINARY CONVERTER
C(3)=110
ADDER
100
REMAPPER
7
i(1)
q(1)
DM
DELAY CIRCUIT
DELAY CIRCUIT
DELAY CIRCUIT
99
91
90
PHASE ROTATION ANGLE JUDGEMENT CIRCUIT 92F
DEMODULATION CIRCUIT 1F
I(8)
Q(8)
SELECTOR
14-1
PHASE ERROR TABLE
15-1
16D
13
66
67
THINNING CIRCUIT
THINNING CIRCUIT
64
65
DIGITAL FILTER
DIGITAL FILTER
CLKSYB
19
SELECTOR
62
63
A/D
A/D
CLKSYB
Δφ(8)
D/A
17
Δφ(3)
LPF
18
60
61
90° PHASE SHIFTER
12
VCO
11
IF
CARRIER REPRODUCTION CIRCUIT 10D

FIG. 9A

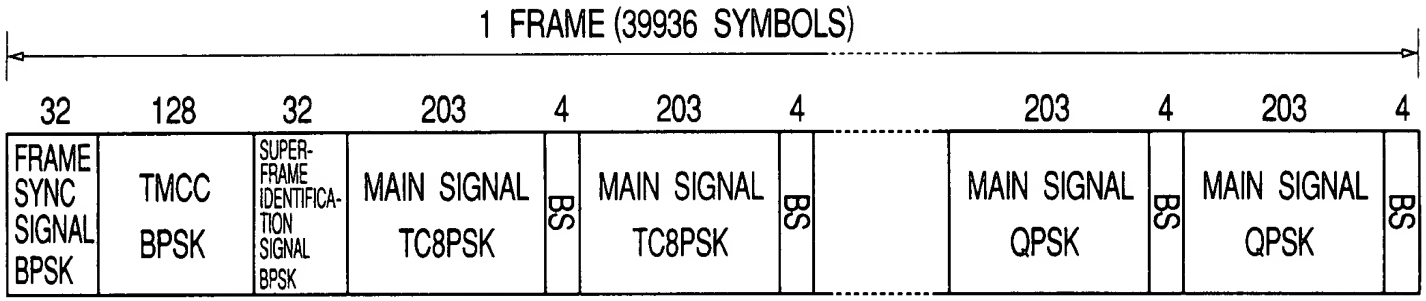

1 FRAME (39936 SYMBOLS)
32
128
32
203
4
203
4
203
4
203
4
FRAME SYNC SIGNAL BPSK
TMCC BPSK
SUPER-FRAME IDENTIFICATION SIGNAL BPSK
MAIN SIGNAL TC8PSK
BS
MAIN SIGNAL TC8PSK
BS
MAIN SIGNAL QPSK
BS
MAIN SIGNAL QPSK
BS

FIG. 9B

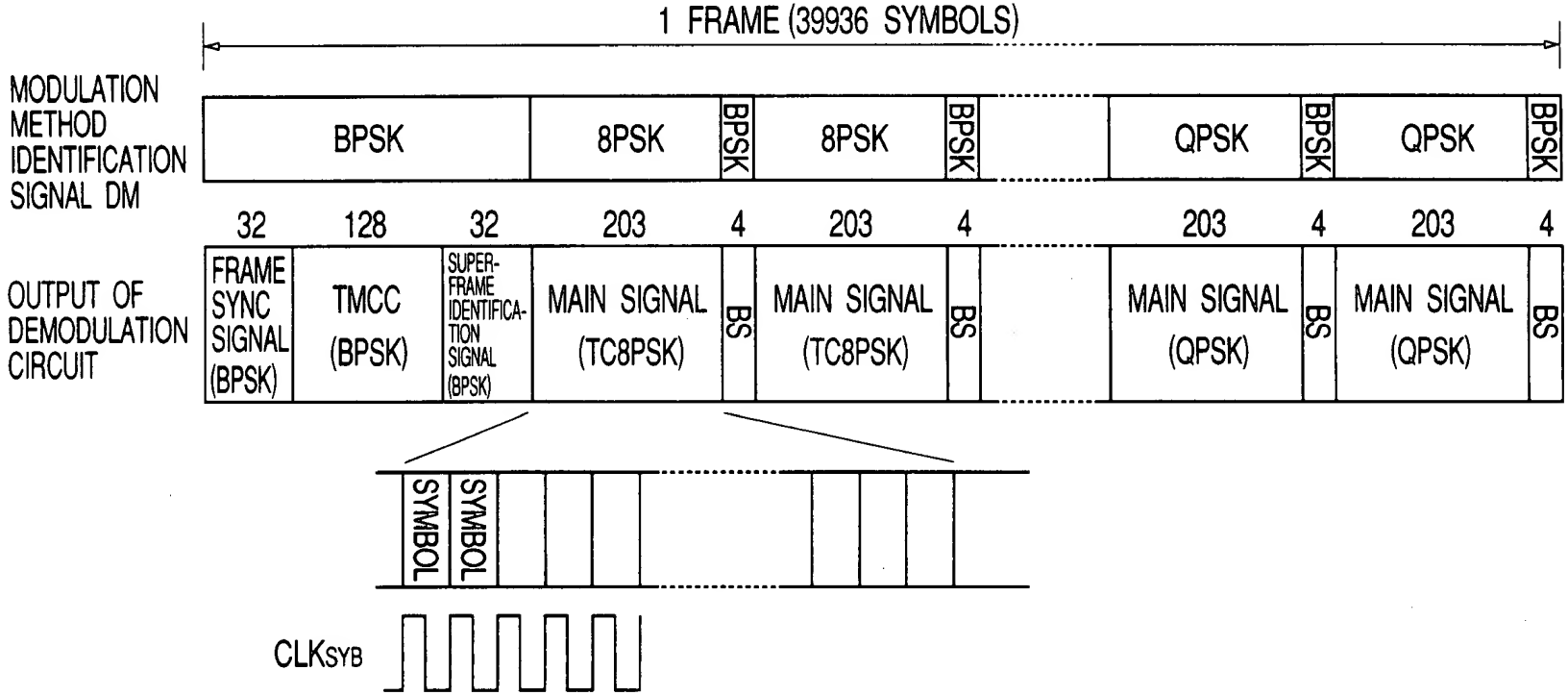

1 FRAME (39936 SYMBOLS)
MODULATION METHOD IDENTIFICATION SIGNAL DM
BPSK
8PSK
BPSK
8PSK
BPSK
QPSK
BPSK
QPSK
BPSK
32
128
32
203
4
203
4
203
4
203
4
OUTPUT OF DEMODULATION CIRCUIT
FRAME SYNC SIGNAL (BPSK)
TMCC (BPSK)
SUPER-FRAME IDENTIFICATION SIGNAL (BPSK)
MAIN SIGNAL (TC8PSK)
BS
MAIN SIGNAL (TC8PSK)
BS
MAIN SIGNAL (QPSK)
BS
MAIN SIGNAL (QPSK)
BS
SYMBOL
SYMBOL
CLKSYB

FIG. 10

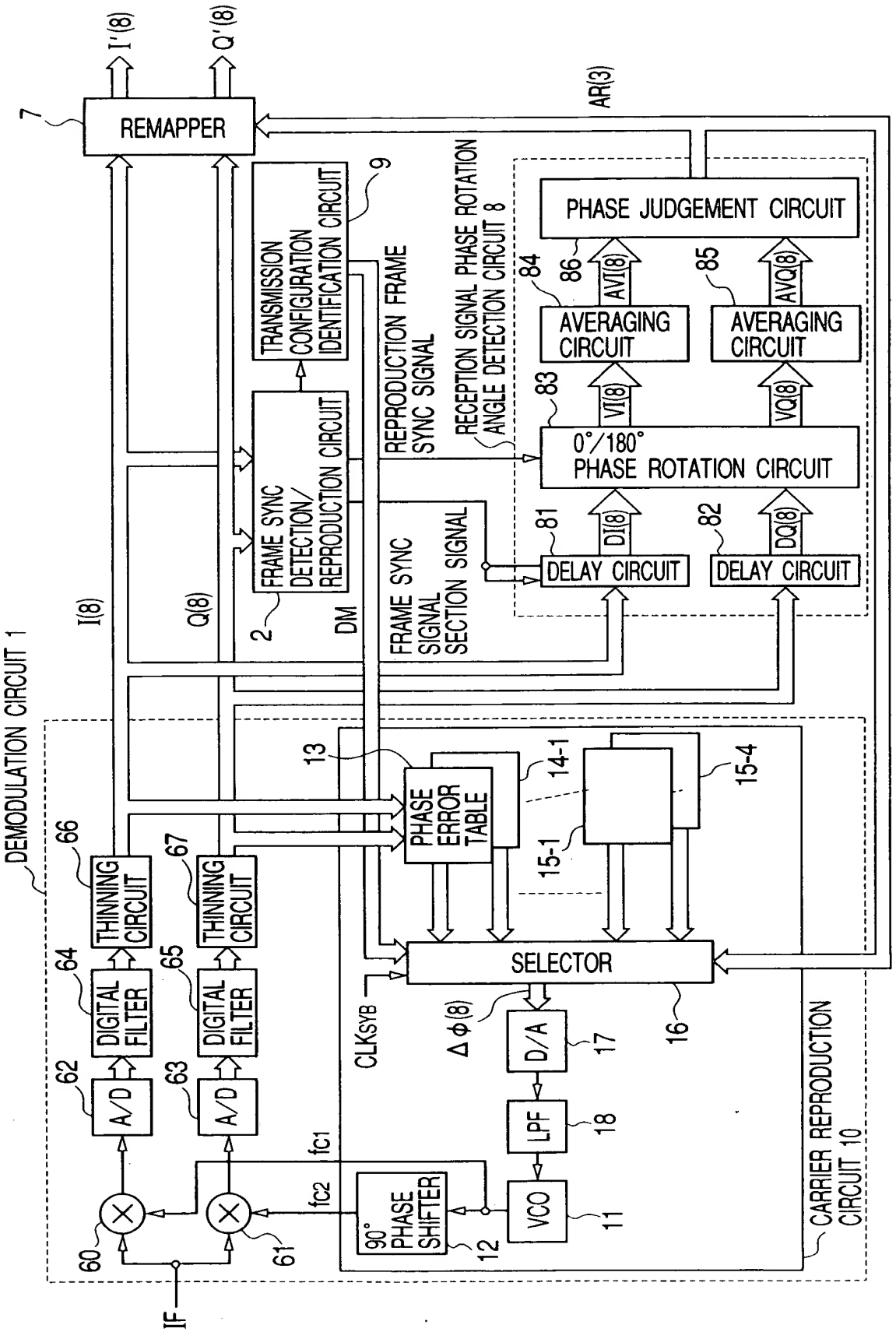

I'(8)
Q'(8)
7
REMAPPER
AR(3)
9
TRANSMISSION CONFIGURATION IDENTIFICATION CIRCUIT
PHASE JUDGEMENT CIRCUIT
84
86
AVI(8)
85
AVQ(8)
AVERAGING CIRCUIT
AVERAGING CIRCUIT
83
VI(8)
VQ(8)
0°/180° PHASE ROTATION CIRCUIT
81
DI(8)
82
DQ(8)
DELAY CIRCUIT
DELAY CIRCUIT
REPRODUCTION FRAME SYNC SIGNAL
RECEPTION SIGNAL PHASE ROTATION ANGLE DETECTION CIRCUIT 8
FRAME SYNC SIGNAL SECTION SIGNAL
FRAME SYNC DETECTION/ REPRODUCTION CIRCUIT
2
DM
I(8)
Q(8)
DEMODULATION CIRCUIT 1
13
PHASE ERROR TABLE
14-1
15-1
15-4
66
67
THINNING CIRCUIT
THINNING CIRCUIT
64
65
DIGITAL FILTER
DIGITAL FILTER
62
63
A/D
A/D
SELECTOR
CLKSYB
Δφ(8)
D/A
17
16
LPF
18
fc1
fc2
90° PHASE SHIFTER
12
VCO
11
60
61
IF
CARRIER REPRODUCTION CIRCUIT 10

FIG. 11A

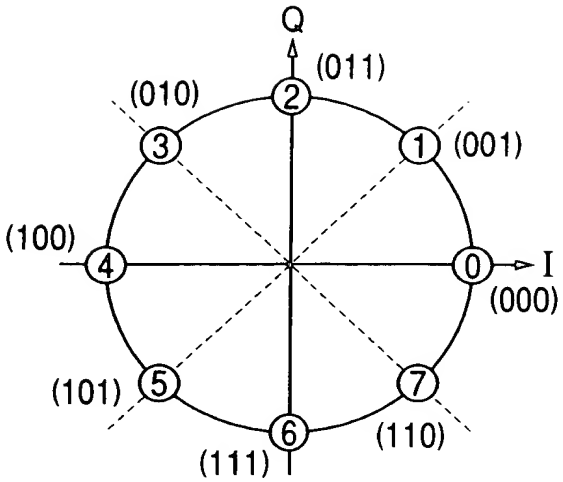


FIG. 11B

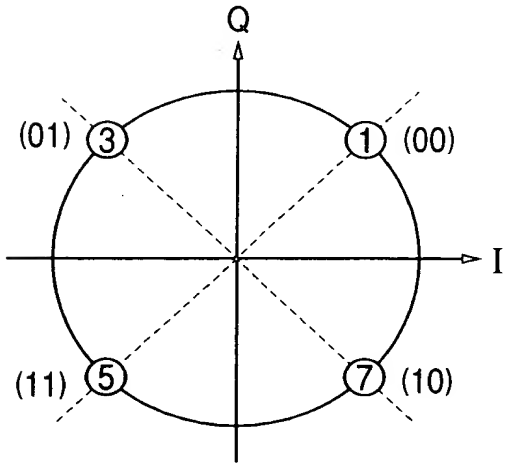


FIG. 11C

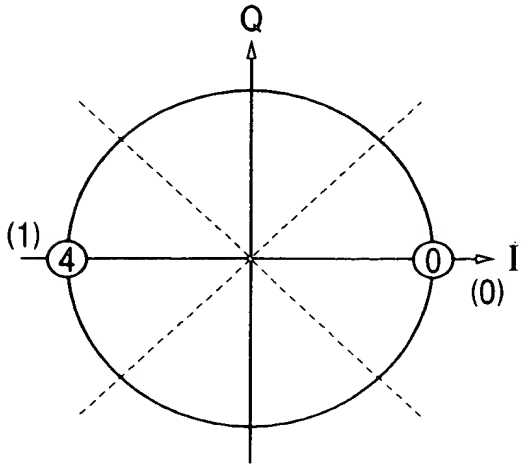


FIG. 12

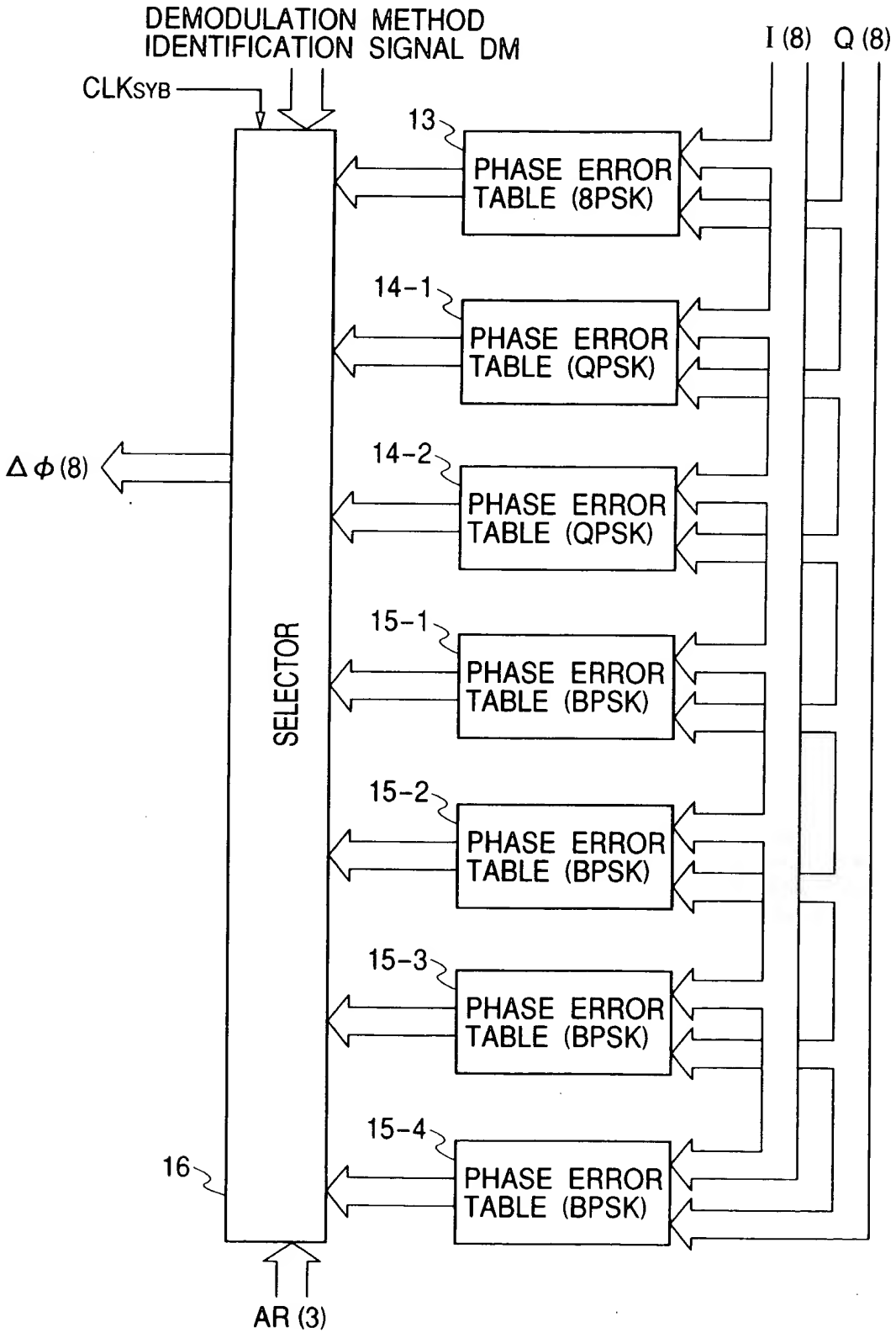

DEMODULATION METHOD IDENTIFICATION SIGNAL DM
CLKSYB
I (8)
Q (8)
13
PHASE ERROR TABLE (8PSK)
14-1
PHASE ERROR TABLE (QPSK)
14-2
PHASE ERROR TABLE (QPSK)
15-1
PHASE ERROR TABLE (BPSK)
15-2
PHASE ERROR TABLE (BPSK)
15-3
PHASE ERROR TABLE (BPSK)
15-4
PHASE ERROR TABLE (BPSK)
SELECTOR
Δφ (8)
16
AR (3)

FIG. 13

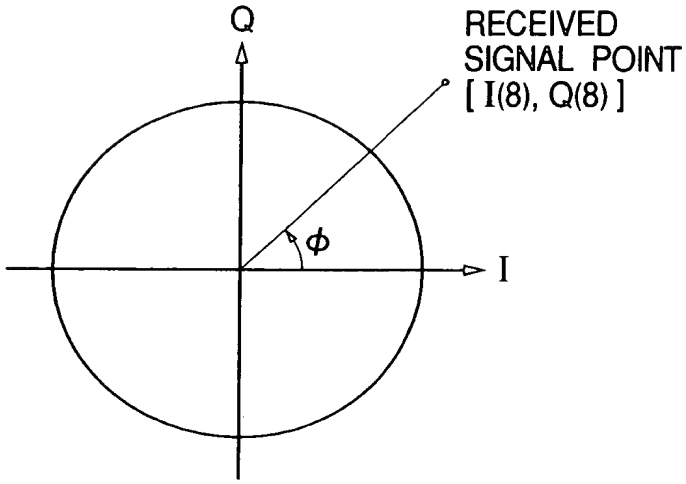

Q
RECEIVED
SIGNAL POINT
[I(8), Q(8)]
ϕ
I

FIG. 14

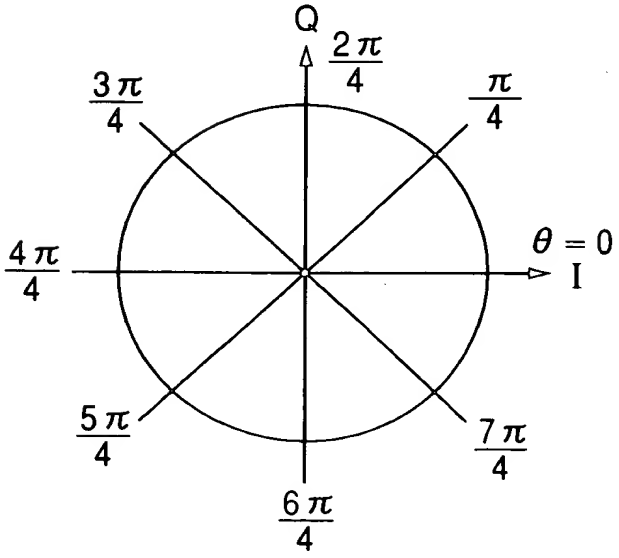

Q
2π/4
3π/4
π/4
4π/4
θ = 0
I
5π/4
7π/4
6π/4

FIG. 15

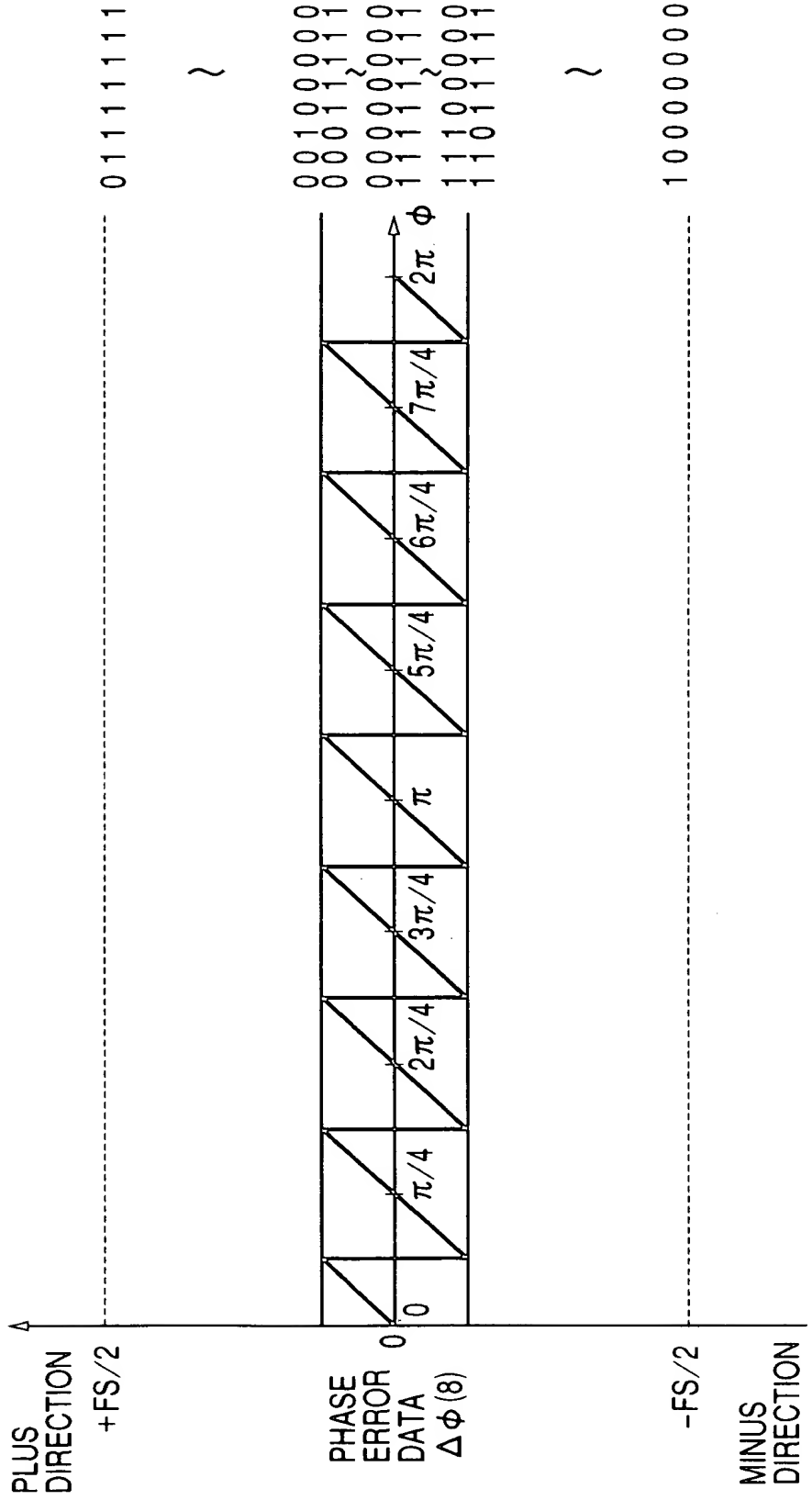

PLUS DIRECTION
+FS/2
PHASE ERROR DATA Δφ(8)
0
-FS/2
MINUS DIRECTION
φ
2π
7π/4
6π/4
5π/4
π
3π/4
2π/4
π/4
0
01111111
00100000
00011111
00000000
11111111
11100000
11011111
10000000

FIG. 16

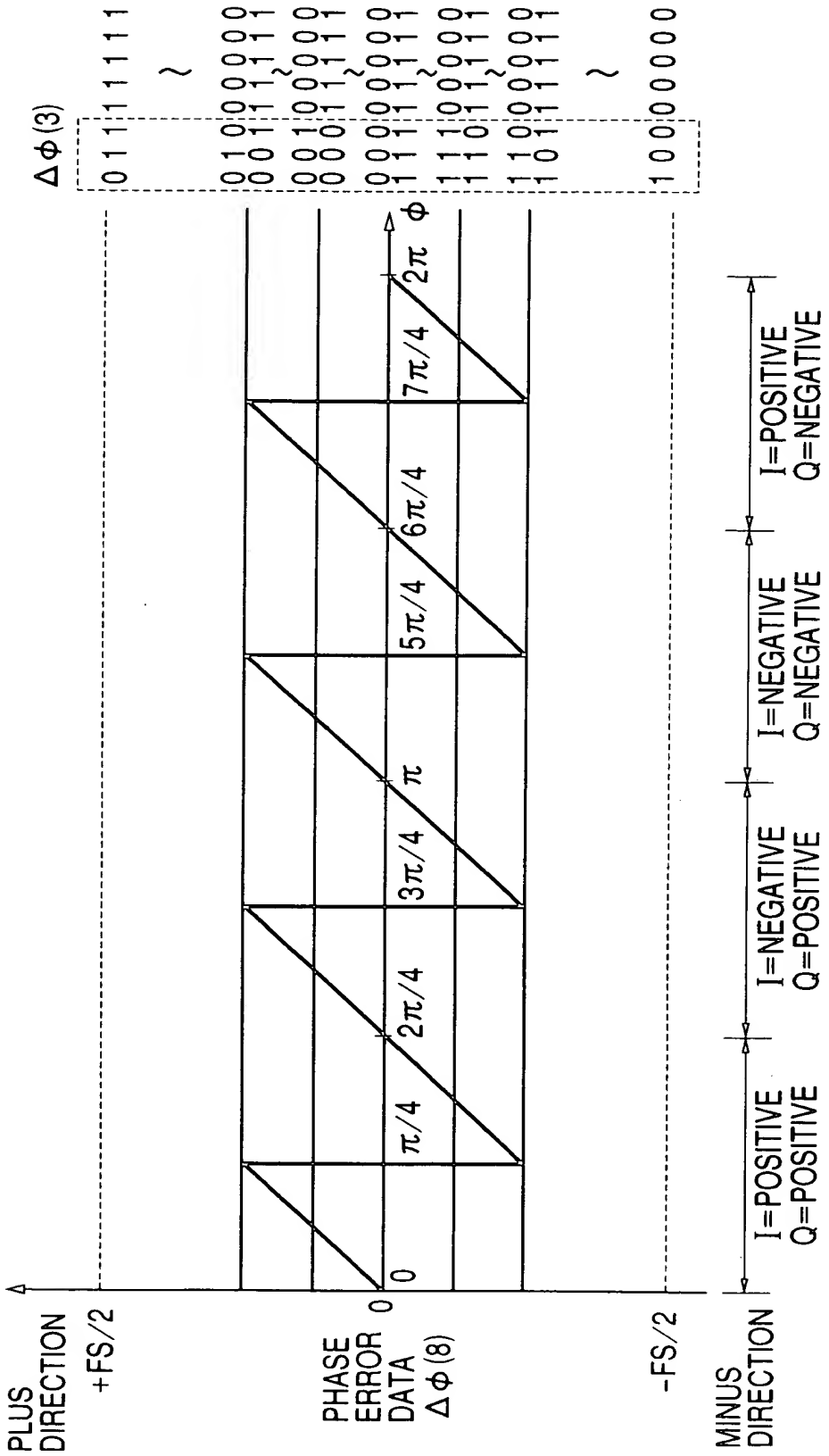

Δφ(3)
PLUS DIRECTION
+FS/2
PHASE ERROR DATA Δφ(8)
0
-FS/2
MINUS DIRECTION
φ
2π
7π/4
6π/4
5π/4
π
3π/4
2π/4
π/4
0
I=POSITIVE Q=POSITIVE
I=NEGATIVE Q=POSITIVE
I=NEGATIVE Q=NEGATIVE
I=POSITIVE Q=NEGATIVE

FIG. 17

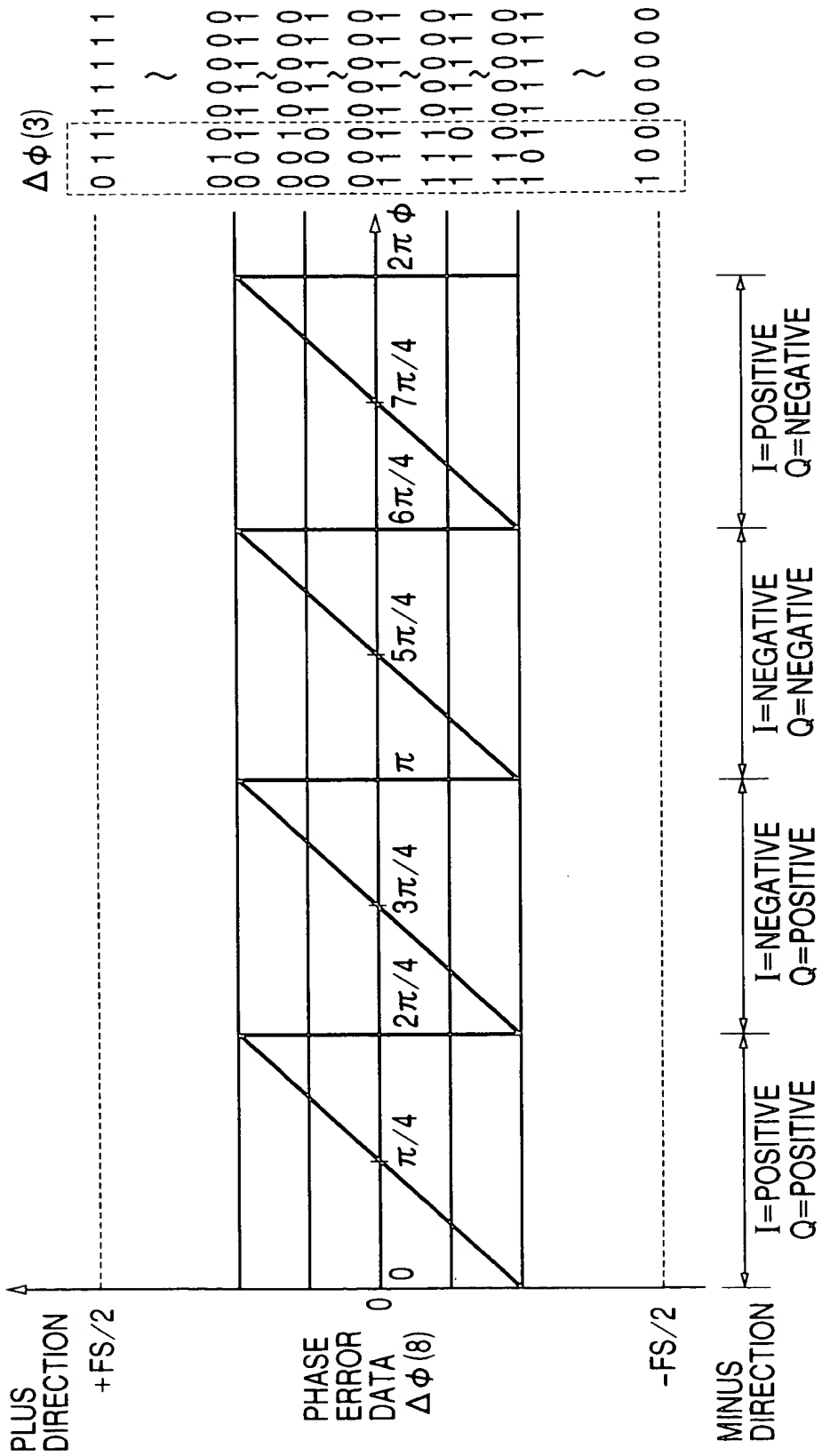

Δφ(3)
0 1 1 1 1 1 1 1
~
0 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1
0 0 0 0 0 0 0 0
0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1
1 0 0 0 0 0 0 0
1 0 0 0 1 1 1 1
1 0 1 1 0 0 1 1
1 1 0 1 0 1 0 1
1 1 1 0 0 0 0 0
1 1 1 0 1 1 1 1
1 1 1 1 0 0 1 1
1 1 0 1 0 1 0 1
~
1 0 0 0 0 0 0 0
PLUS DIRECTION
+FS/2
0
-FS/2
MINUS DIRECTION
PHASE ERROR DATA Δφ(8)
2πφ
0
π/4
2π/4
3π/4
π
5π/4
6π/4
7π/4
I=POSITIVE Q=POSITIVE
I=NEGATIVE Q=POSITIVE
I=NEGATIVE Q=NEGATIVE
I=POSITIVE Q=NEGATIVE

FIG. 18

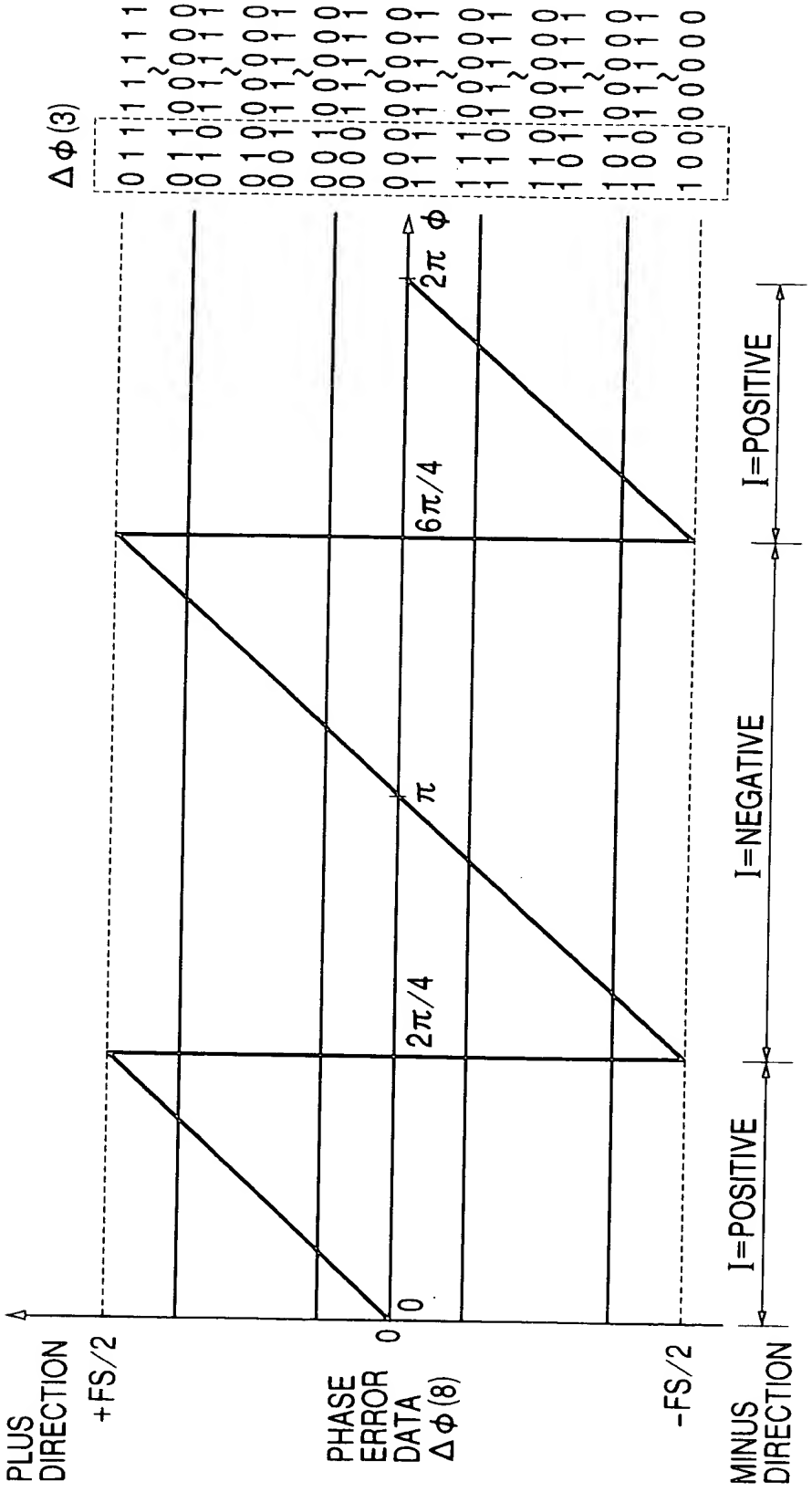

Δφ(3)
0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
0 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0
0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
PLUS DIRECTION
+FS/2
0
-FS/2
MINUS DIRECTION
PHASE ERROR DATA Δφ(8)
2π φ
6π/4
π
2π/4
0
I=POSITIVE
I=NEGATIVE
I=POSITIVE

FIG. 19

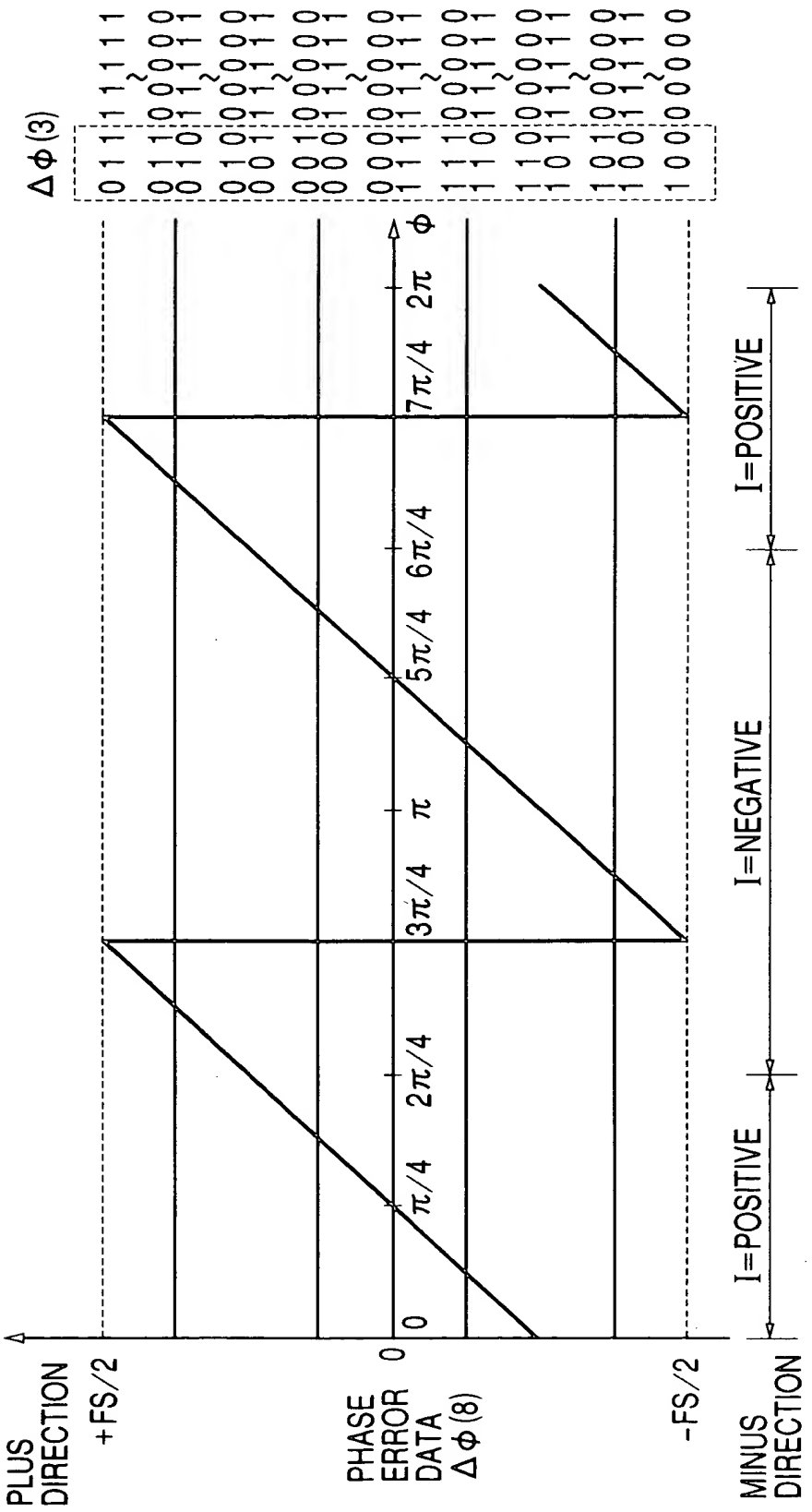

Δφ(3)
PLUS DIRECTION
+FS/2
PHASE ERROR DATA Δφ(8)
0
-FS/2
MINUS DIRECTION
I=POSITIVE
I=NEGATIVE
I=POSITIVE
0
π/4
2π/4
3π/4
π
5π/4
6π/4
7π/4
2π
φ

FIG. 20

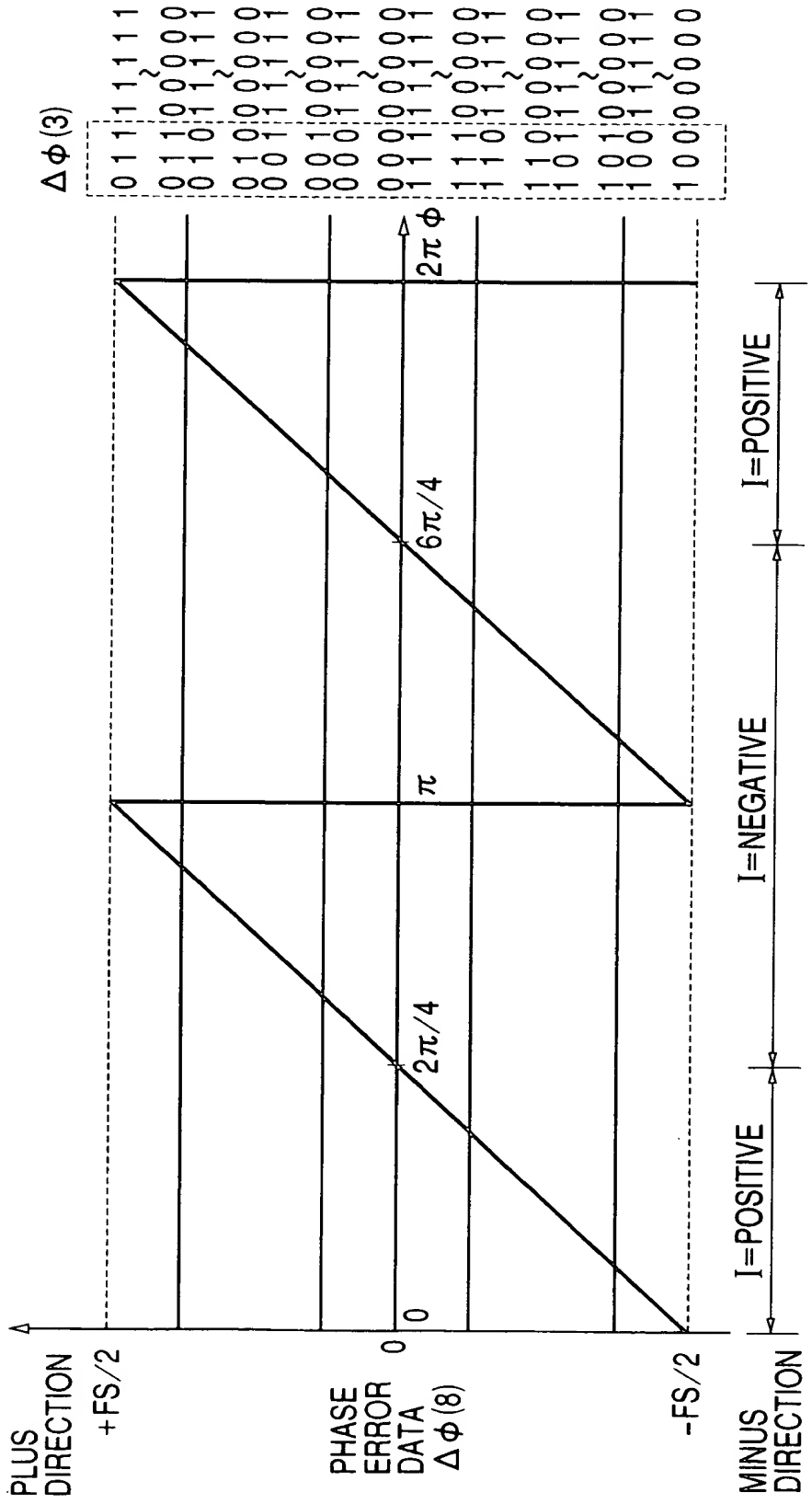

Δφ(3)
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1
0 0 0 0 1 1 0 0 1 1 0 0 1 1 0 0
0 0 0 0 0 1 1 0 0 1 1 0 0 1 1 0
0 0 0 0 0 0 1 1 0 0 1 1 0 0 1 1
0 0 0 0 0 0 0 1 1 0 0 1 1 0 0 0
0 0 0 0 0 0 0 0 1 1 0 0 1 1 1 1
2π φ
6π/4
π
2π/4
0
PLUS DIRECTION
+FS/2
PHASE ERROR DATA Δφ(8)
0
-FS/2
MINUS DIRECTION
I=POSITIVE
I=NEGATIVE
I=POSITIVE

FIG. 21

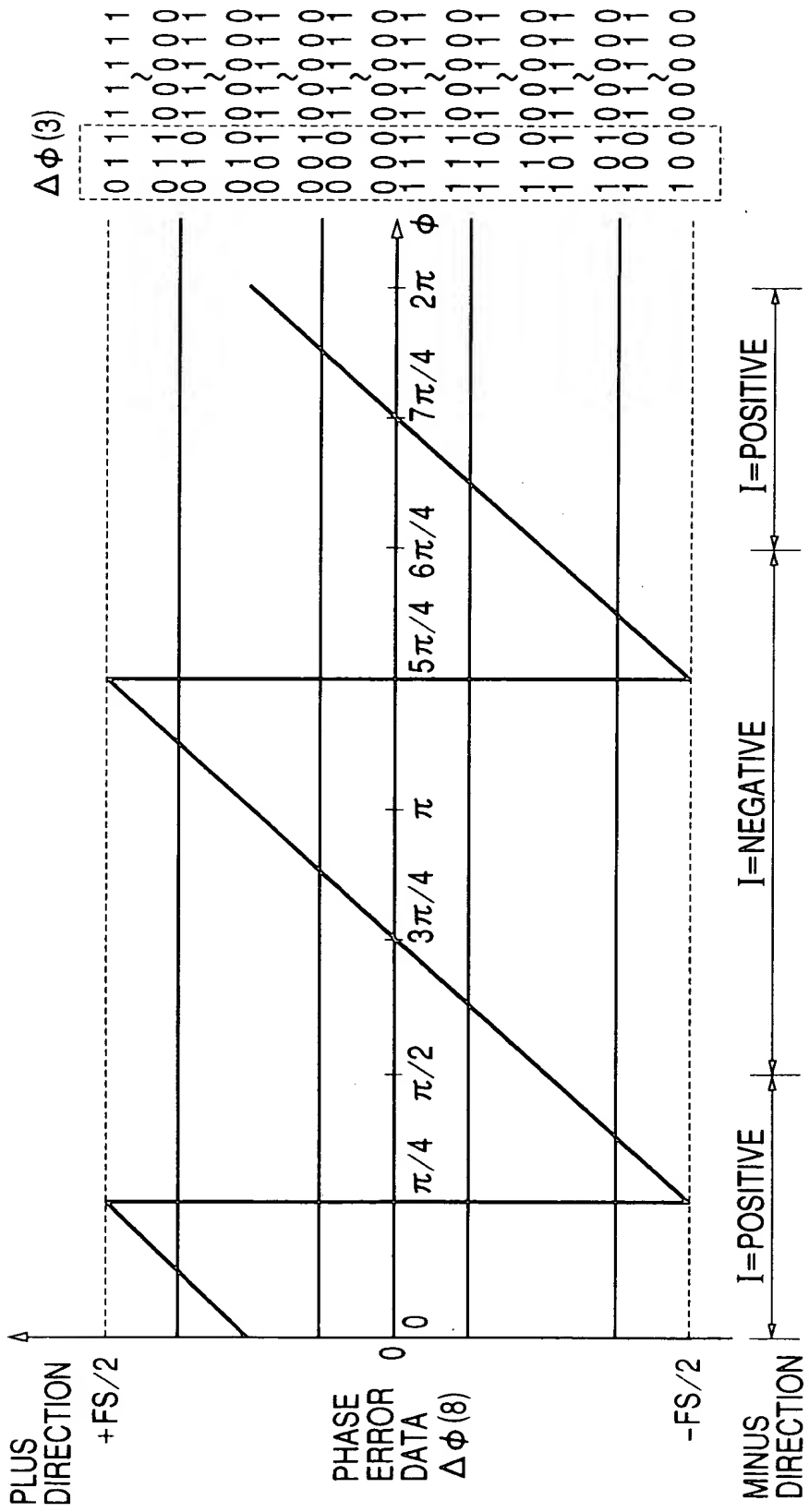

Δφ(3)
PLUS DIRECTION
+FS/2
0
-FS/2
MINUS DIRECTION
PHASE ERROR DATA Δφ(8)
π/4
π/2
3π/4
π
5π/4
6π/4
7π/4
2π
φ
I=POSITIVE
I=NEGATIVE
I=POSITIVE

FIG. 22

FRAME SYNC DETECTION/REPRODUCTION CIRCUIT 2

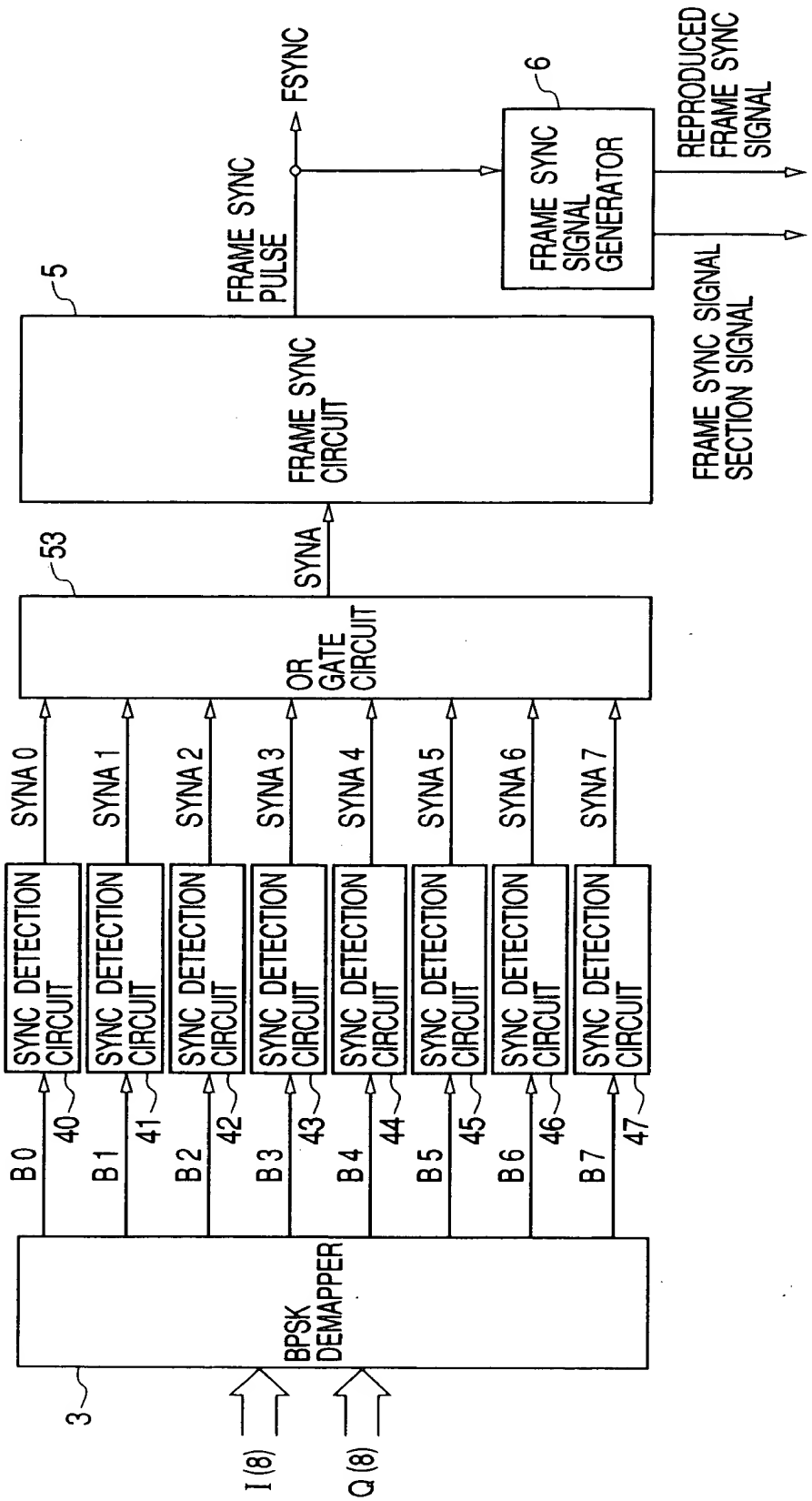


FIG. 23A

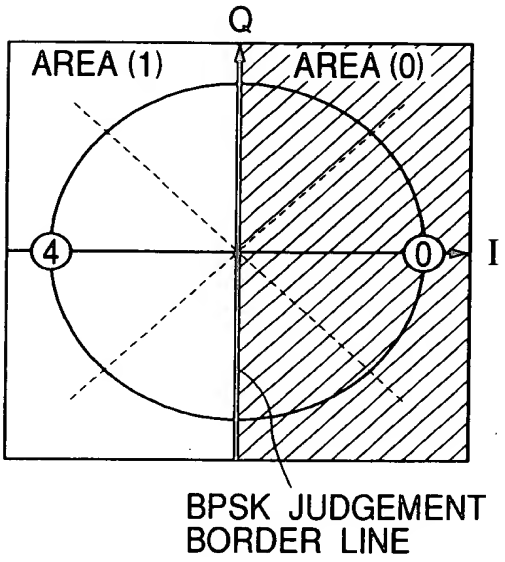


FIG. 23B

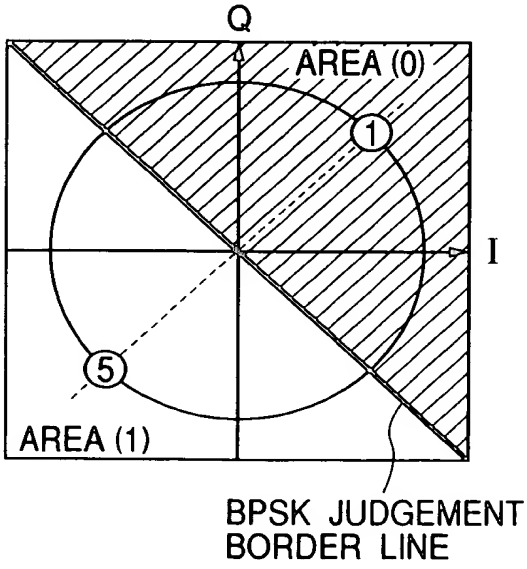


FIG. 24

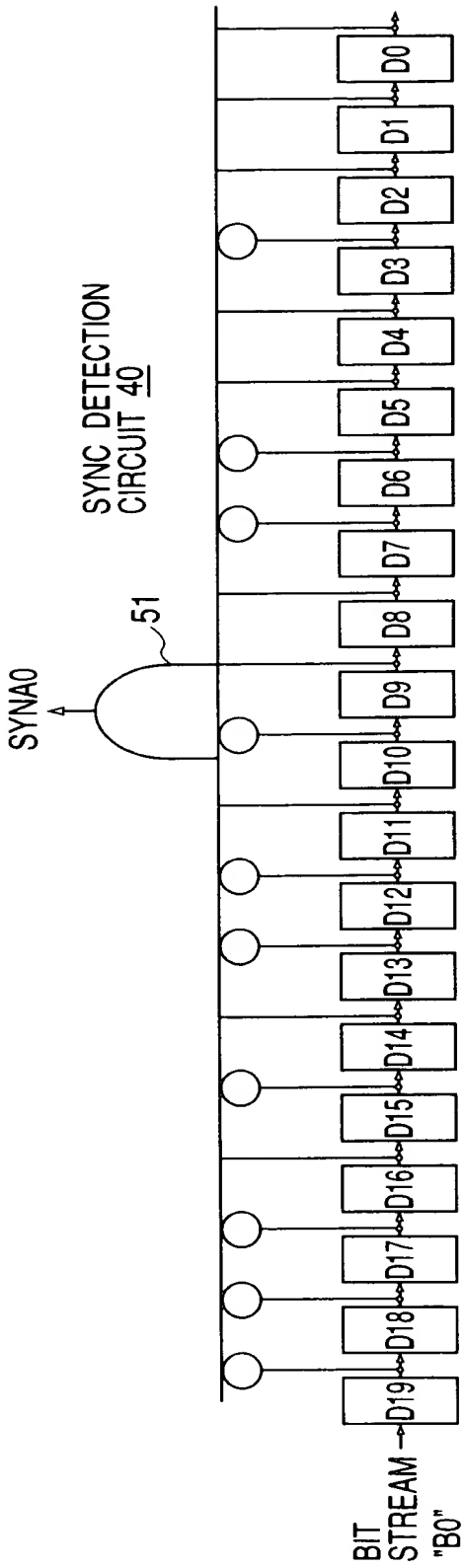

SYNC DETECTION CIRCUIT 40
51
SYNA0
BIT STREAM "B0"
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19

FIG. 25

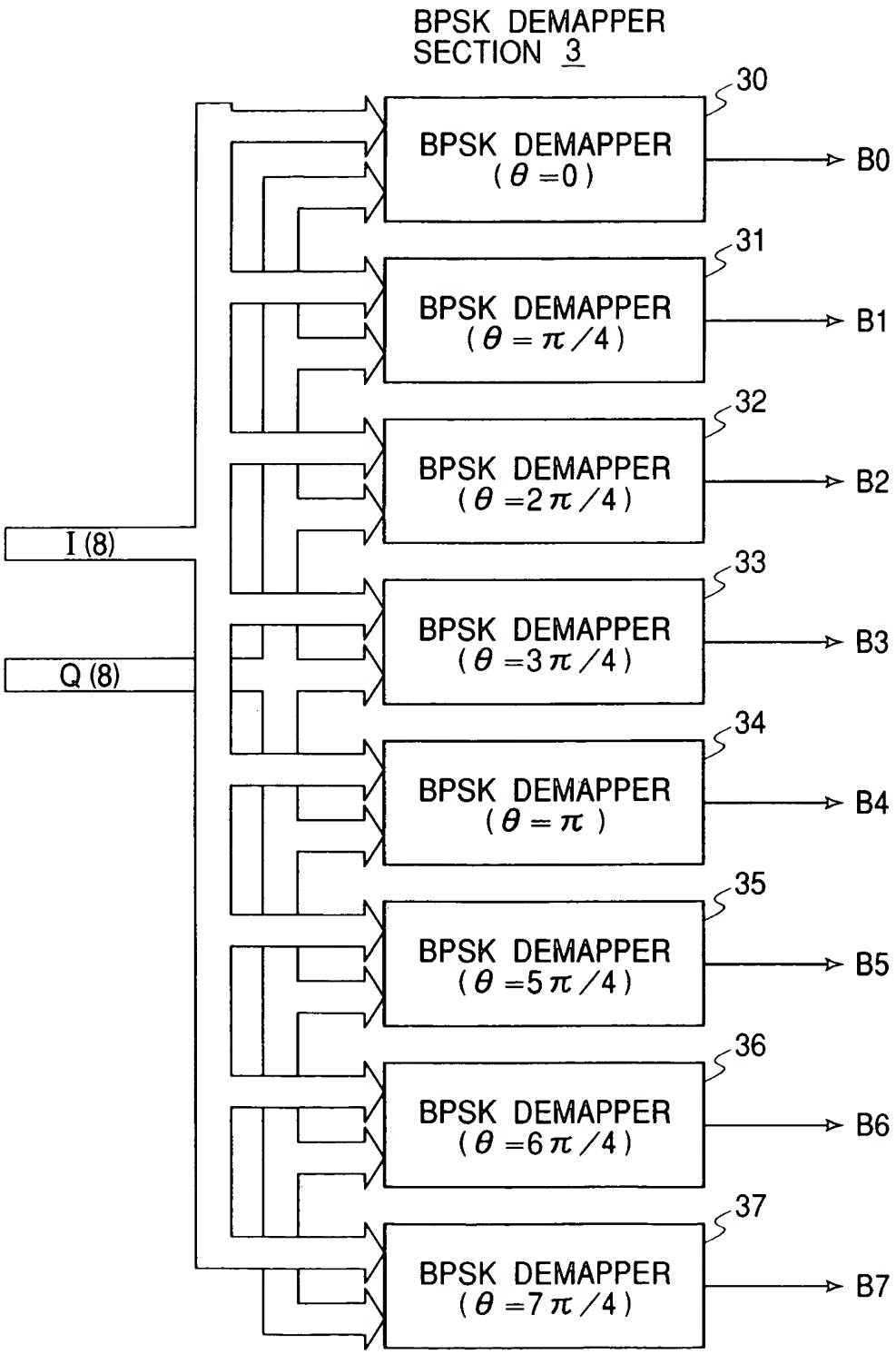

BPSK DEMAPPER
SECTION 3
30
BPSK DEMAPPER
(θ =0)
B0
31
BPSK DEMAPPER
(θ = π /4)
B1
32
BPSK DEMAPPER
(θ =2π /4)
B2
33
BPSK DEMAPPER
(θ =3π /4)
B3
34
BPSK DEMAPPER
(θ = π)
B4
35
BPSK DEMAPPER
(θ =5π /4)
B5
36
BPSK DEMAPPER
(θ =6π /4)
B6
37
BPSK DEMAPPER
(θ =7π /4)
B7
I (8)
Q (8)

FIG. 26A

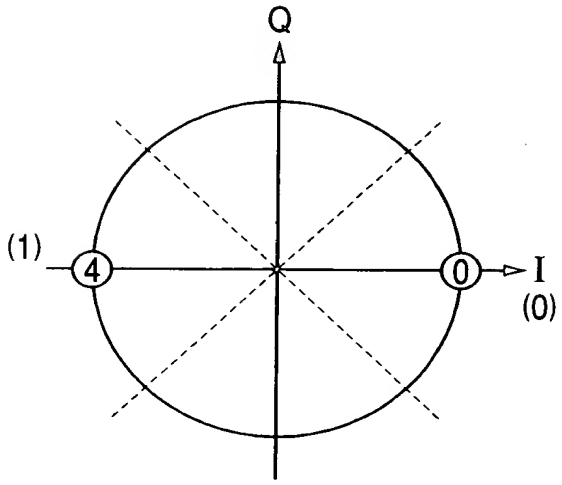


FIG. 26B

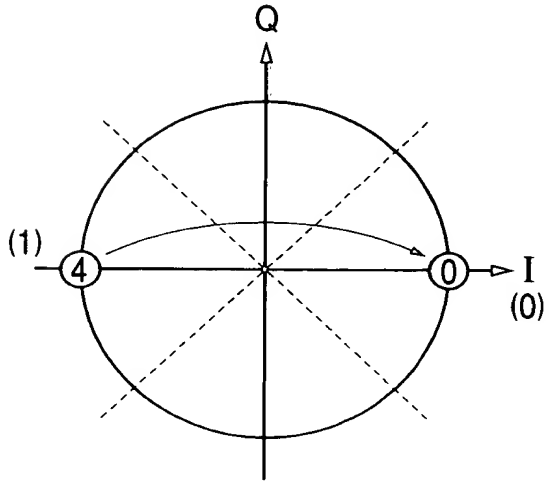
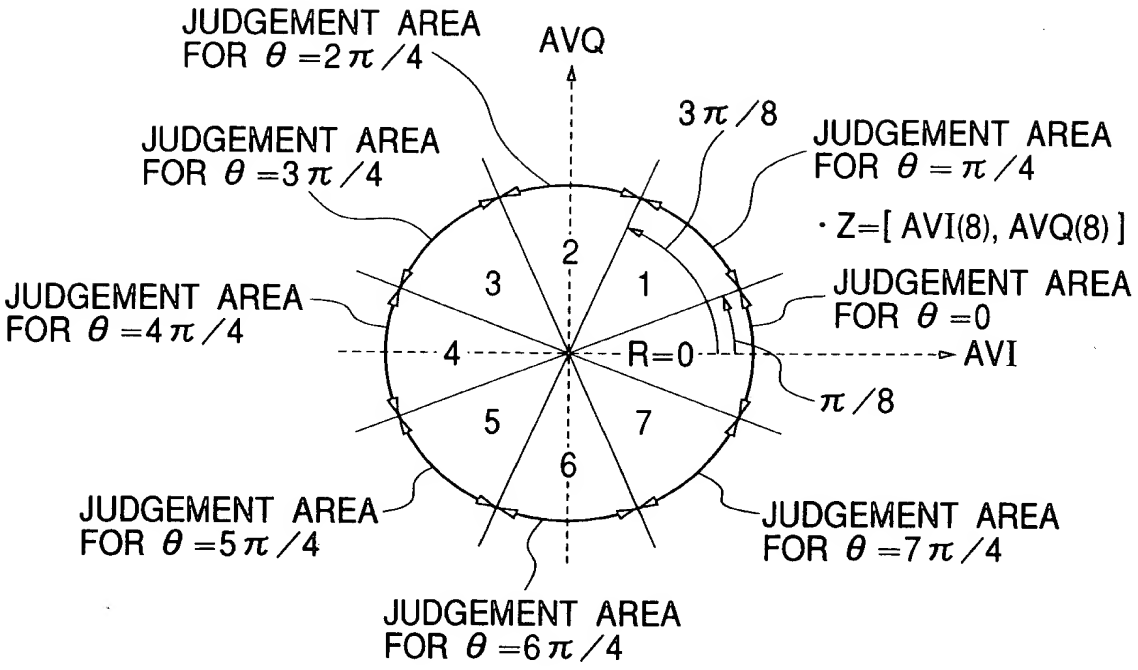


FIG. 27


JUDGEMENT AREA FOR θ =2π/4
AVQ
3π/8
JUDGEMENT AREA FOR θ =π/4
JUDGEMENT AREA FOR θ =3π/4
· Z=[AVI(8), AVQ(8)]
2
3
1
JUDGEMENT AREA FOR θ =4π/4
JUDGEMENT AREA FOR θ =0
4
R=0
AVI
π/8
5
7
6
JUDGEMENT AREA FOR θ =5π/4
JUDGEMENT AREA FOR θ =7π/4
JUDGEMENT AREA FOR θ =6π/4